UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,430	07/29/2003	Jae-Hyoung Choi	5649-1112	6037

20792 7590 08/26/2005

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,430	CHOI ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 33-44* is/are pending in the application.

4a) Of the above claim(s) *2,5-8,16,17,19,20,34 and 35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-4, 9-15, 18, 21-23,33,36-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 42, 43, and 44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 42, 43, and 44 recite "performing a thermal process", in line 2 of each claim. The examiner notes that a thermal process has already been recited in the claims (1, 15, and 33, respectively) from which claims 42, 43, and 44 depend from. Therefore, by reciting "a thermal process" it is not clear if Applicant is referring to the thermal process previously recited in claims 1, 15, and 33 respectively, or if it is referring to an additional thermal process. The examiner suggests amending the claim to recite "the thermal process".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 9, 10, 11, 13, 14, 15, 21, 22, 42, and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art (AAPA, see Figures 1A-1B and Spec. pages 1-2).

AAPA disclose a method for fabricating a semiconductor device, the method comprising:

forming a first conductive layer (20) for a first electrode on a semiconductor substrate;.

forming a dielectric layer (30) on the first conductive layer;

forming a second conductive layer (40) for a second electrode on the dielectric layer;

after forming the dielectric layer and after forming the second conductive layer, removing portions of the second conductive layer and the dielectric layer (see Spec. page 2, lines 15-20); and

performing a thermal process on the second conductive layer and the dielectric layer at a temperature of at least about 400°C (see Spec, page 2, lines 17-22).

In re claim 9, AAPA disclose the method wherein the first conductive layer comprises at leastonematerial selected from the group consisting of platinum, ruthenium, iridium, rhodium, and/or osmium (see Spec., page 2, lines 1-5).

In re claim 10, AAPA disclose the method wherein the second conductive layer comprises a same material as the first conductive layer (see Spec, page 2, lines 14-17).

In re claim 11, AAPA disclose the method wherein forming the dielectric layer comprises forming a tantalum oxide layer (see Spec, page 2, lines 3-14).

In re claim 13, AAPA disclose the method of wherein removing portions of the second conductive layer and the dielectric layer comprises dry etching the second conductive layer and the dielectric (see Spec, page 2, lines 15-18).

In re claim 14, AAPA disclose the method wherein performing the thermal process comprises performing the thermal process on the second conductive layer and the dielectric layer after removing portions of the second conductive layer and the dielectric layer (see Spec, page 2, lines 18-21).

In re claim 42, AAPA disclose the method wherein performing a thermal process comprises performing a thermal process after removing portions of the second conductive layer and after removing portions of the dielectric layer (see Spec, page 2, lines 18-21).

In re claim 15, AAPA disclose the method for fabricating a semiconductor device, the method comprising:

forming a first conductive layer (20) for a first electrode on a semiconductor substrate;

forming a tantalum oxide layer (30) on the first conductive layer;

forming a second conductive layer (40) for a second electrode on the tantalum oxide layer;

after forming the tantalum oxide layer and after forming the second conductive layer, removing portions of the second conductive layer and portions of the tantalum oxide layer (see Spec. page 2, lines 15-20); and

performing a thermal process to reduce an interface stress between the second conductive layer and the tantalum oxide layer and to cure the tantalum oxide layer,

while maintaining the tantalum oxide layer in a substantially amorphous state during and after the thermal process (see Spec, page 2, lines 17-22).

In re claim 21, AAPA disclose the method wherein the first conductive layer comprises at leastonematerial selected from the group consisting of platinum, ruthenium, iridium, rhodium, and/or osmium (see Spec, page 2, lines 1-5).

In re claim 22, AAPA disclose the method wherein the second conductive layer comprises a same material as the first conductive layer (see Spec, page 2, lines 14-17).

In re claim 43, AAPA disclose the method wherein performing a thermal process comprises performing a thermal process after removing portions of the second conductive layer and after removing portions of the dielectric layer (see Spec, page 2, lines 18-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 12, 18, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see Figures 1A-1B and Spec. pages 1-2) in view of Narwankar et al. (U.S. Patent No. 6,475,854).

In re claims 4 and 18, AAPA discloses the method of performing a thermal process at a temperature of about 400 °C in an oxygen atmosphere, but does not disclose the method wherein the performing the thermal process comprises heating the dielectric layer and the second conductive layer at a temperature in the range of about 450°C to 600°C in an inert gas atmosphere

Narwankar et al. disclose the method wherein the performing the thermal process comprises heating the dielectric layer and the second conductive layer at a temperature in the range of about 450°C to 600°C in an oxygen atmosphere or an inert gas atmosphere (see column 15, lines 55-60, column 11, lines 4-10, and column 9, lines 10-24 and Table 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the thermal process of AAPA by the method of Narwankar et al. because as Narwankar et al. teaches while annealing the top electrode and dielectric, a pure oxygen atmosphere is interchangeable with an atmosphere with inert gas (see Table 1) and that the annealing allows for incorporation of oxygen within the electrode which provides for improved performance of the capacitor (see column 1,, lines 5-15 and column 15, lines 35-55).

In re claims 12 and 23, AAPA discloses the method of forming a capacitor including the method of forming the dielectric layer of a tantalum oxide, but does not disclose the method wherein forming the dielectric layer comprises depositing tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD.

Narwankar et al. disclose the method wherein forming the dielectric layer comprises depositing tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD (see column 15, lines 15-25 and Table I).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD because while Narwankar teaches that many deposition methods may be used (see column 10, lines 30-40 and Table 1), Narwankar et al. teaches that CVD and the claimed temperature range are preferred. Further, CVD is a preferred method of depositing tantalum oxide in capacitor formation because it allows for conformal coverage in high aspect ratio vias, which allow for increased capacitance.

Claims 4, 12, 18, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see Figures 1A-1B and Spec. pages 1-2) in view of Lin et al. (U.S. Patent Appl. 2003/0107076).

In re claims 4 and 18, AAPA discloses the method of performing a thermal process at a temperature of about 400 °C in an oxygen atmosphere, but does not disclose the method wherein the performing the thermal process comprises heating the dielectric layer and the second conductive layer at a temperature in the range of about 450°C to 600°C in an inert gas atmosphere

Lin et al. disclose the method wherein the performing the thermal process comprises heating the dielectric layer and the second conductive layer at a temperature

in the range of about 450°C to 600°C in an oxygen atmosphere or an inert gas atmosphere (see [0098])

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the thermal process of AAPA by the method of Lin et al. because as Lin et al. teaches the method reduces the damage to the capacitors in the back end process before interconnections are made (see [0098]).

In re claims 12 and 23, AAPA discloses the method of forming a capacitor including the method of forming the dielectric layer of a tantalum oxide, but does not disclose the method wherein forming the dielectric layer comprises depositing tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD.

Lin et al. disclose the method wherein forming the dielectric layer comprises depositing tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD (see [0088]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD because CVD is a preferred method of depositing tantalum oxide in capacitor formation because it allows for conformal coverage in high aspect ratio vias, which allow for increased capacitance.

Claims 33, 36-39, 41 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see Figures 1A-1B and Spec. pages 1-2) in view of Kunitomo et al. (U.S. Patent No. 6,235,572)

In re claim 33, AAPA disclose the method for fabricating a semiconductor device, the method comprising:

forming a first conductive layer (20) for a first electrode on a semiconductor substrate;

forming a tantalum oxide layer (30) on the first conductive layer;

forming a second conductive layer (40) for a second electrode on the tantalum oxide layer;

after forming the tantalum oxide layer and after forming the second conductive layer, removing portions of the second conductive layer and portions of the tantalum oxide layer (see Spec. page 2, lines 15-20); and

performing a thermal process to reduce an interface stress between the second conductive layer and the tantalum oxide layer and to cure the tantalum oxide layer (see Spec, page 2, lines 17-22).

Narwankar et al. disclose the method as claimed and rejected above, but does not disclose the method of forming the dielectric layer by the method of depositing a seed layer on the first conductive layer, and crystallizing the seed layer. Kunitomo et al. disclose the method of forming the dielectric layer by the method of depositing a seed layer on the first conductive layer, and crystallizing the seed layer (see column 18, line 28 through column 20 line 5). It would have been obvious to one of ordinary skill in the

art at the time the invention was made to form the tantalum oxide layer by depositing a seed layer on the first conductive layer, and crystallizing the seed layer, because as Kunitomo et al. teach, it reduces stress of the crystallized tantalum oxide fill, improves morphology and density, and further reduces the leakage current of the dielectric (see column 19, lines 40-45, and column 20, lines 1-25).

In re claim 36, the combined AAPA and Kunitomo et al. disclose the method wherein forming the seed layer comprises forming a seed layer having a thickness in the range of about 30A to 60A (see Kunitomo column 18, lines 38-45). Kunitomo et al. disclose the method of forming the seed layer to a thickness of 10nm or less, which is 100 Angstroms or less. The examiner considers 100 Angstroms or less to read on about 60 Angstroms.

The examiner notes that Applicant does not teach that the thickness range solves any stated problem or is for any particular purpose. Therefore, the thickness range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the seed layer to a thickness of about 30 to about 60 angstroms, since the tantalum oxide layer would have functioned as a seed layer to allow further growth of the layer, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 37, the combined AAPA and Kunitomo et al. disclose the method wherein crystallizing the seed layer comprises heating the seed layer at a temperature in the range of 650°C to 750°C (see Kunitomo et al. column 18, line 45 through column 19, line 15).

In re claim 38, AAPA disclose the method wherein the first conductive layer comprises at least one material selected from the group consisting of platinum, ruthenium, iridium, rhodium, and/or osmium (see Spec., page 2, lines 1-5).

In re claim 39, AAPA disclose the method wherein the second conductive layer comprises a same material as the first conductive layer (see Spec, page 2, lines 14-17).

In re claim 41, the combined AAPA and Kunitomo et al. disclose the method wherein the seed layer comprises forming a seed layer of a tantalum oxide layer (see Kunitomo et al. column 18, line 28 through column 20 line 5).

In re claim 44, AAPA disclose the method wherein performing a thermal process comprises performing a thermal process after removing portions of the second conductive layer and after removing portions of the dielectric layer (see Spec, page 2, lines 18-21).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see Figures 1A-1B and Spec. pages 1-2) in view of Narwankar et al. (U.S. Patent No. 6,475,854) and further in view of Kunitomo et al. (U.S. Patent No. 6,235,572)

In re claim 3, AAPA and Narwankar et al. disclose the method as claimed and rejected above, but do not disclose the method of forming the dielectric layer by the method of depositing a seed layer on the first conductive layer, and crystallizing the seed layer. Kunitomo et al. disclose the method of forming the dielectric layer by the method of depositing a seed layer on the first conductive layer, and crystallizing the seed layer (see column 18, line 28 through column 20 line 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the tantalum oxide layer by depositing a seed layer on the first conductive layer, and crystallizing the seed layer, because as Kunitomo et al. teach, it reduces stress of the crystallized tantalum oxide fill, improves morphology and density, and further reduces the leakage current of the dielectric (see column 19, lines 40-45, and column 20, lines 1-25).

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see Figures 1A-1B and Spec. pages 1-2) in view of Kunitomo et al. (U.S. Patent No. 6,235,572) and further in view of Narwankar et al. (U.S. Patent No. 6,475,854).

In re claim 40, AAPA and Kunitomo et al. discloses the method of forming a capacitor including the method of forming the dielectric layer of a tantalum oxide, but does not disclose the method wherein forming the dielectric layer comprises depositing tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD.

Narwankar et al. disclose the method wherein forming the dielectric layer comprises depositing tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD (see column 15, lines 15-25 and Table I).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD because while Narwankar teaches that many deposition methods may be used (see column 10, lines 30-40 and Table 1), Narwankar et al. teaches that CVD and the claimed temperature range are preferred. Further, CVD is a preferred method of depositing tantalum oxide in capacitor formation because it allows for conformal coverage in high aspect ratio vias, which allow for increased capacitance.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see Figures 1A-1B and Spec. pages 1-2) in view of Lin et al. (U.S. Patent Appl. 2003/0107076) and further in view of Kunitomo et al. (U.S. Patent No. 6,235,572)

In re claim 3, AAPA and Lin et al. disclose the method as claimed and rejected above, but does not disclose the method of forming the dielectric layer by the method of depositing a seed layer on the first conductive layer, and crystallizing the seed layer. Kunitomo et al. disclose the method of forming the dielectric layer by the method of depositing a seed layer on the first conductive layer, and crystallizing the seed layer (see column 18, line 28 through column 20 line 5). It would have been obvious to one

of ordinary skill in the art at the time the invention was made to form the tantalum oxide layer by depositing a seed layer on the first conductive layer, and crystallizing the seed layer, because as Kunitomo et al. teach, it reduces stress of the crystallized tantalum oxide fill, improves morphology and density, and further reduces the leakage current of the dielectric (see column 19, lines 40-45, and column 20, lines 1-25).

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see Figures 1A-1B and Spec. pages 1-2) in view of Kunitomo et al. (U.S. Patent No. 6,235,572) and further in view of Lin et al. (U.S. Patent Appl. 2003/0107076)

In re claim 40, AAPA and Kunitomo et al. discloses the method of forming a capaicitor including the method of forming the dielectric layer of a tantalum oxide, but does not disclose the method wherein forming the dielectric layer comprises depositing tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD.

Lin et al. disclose the method wherein forming the dielectric layer comprises depositing tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD (see [0088]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the tantalum oxide at a temperature in the range of about 350°C to 500°C using CVD because CVD is a preferred method of depositing tantalum

oxide in capacitor formation because it allows for conformal coverage in high aspect ratio vias, which allow for increased capacitance.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-4, 9-15, 18, 21-23, 33, 36-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk